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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/002,265	12/31/97	VAN DER WAL G	DSRC-0005/SA

LM02/0902

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ART UNIT	**PAPER NUMBER**
2711	8

DATE MAILED: 09/02/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/002,265	Van Der Wal
Examiner	**Group Art Unit**
Reuben M. Brown	2711

☒ Responsive to communication(s) filed on *Jun 7, 1998* .

☒ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-30* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-30* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *5*

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4 & 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, with respect to the claimed "dual image pointwise video processing operation", it is unclear as to whether applicant is claiming that two separate image streams or sources are concurrently processed, or that dual portions of a single image are concurrently processed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

4. Claims 1-3, 20, 21, 22, 24, 25, 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Gove, (U.S. Pat # 5,768,609).

Considering claim 1, Gove discloses all subject matter including at least processing module containing at least one general purpose microprocessor, as a plurality of image processing systems, i.e. ISP nodes 30-32 are disclosed, wherein each image processing system comprises a master processor 12, which controls hardware and software operation of the video processing system using control data, and which also processes video data, (Fig. 1; Fig. 3; col. 8, lines 51-65; col. 13, lines 20-60; col. 14, lines 56-68; col. 16, lines 3-7). The claimed video processing module which contains parallel pipelined video hardware components, wherein the video processing

module is responsive to the control data to perform different video processing operations on the video data is met by the parallel processors 100-10n, (col. 9, lines 47-57; col. 13, lines 51-67; col. 14, lines 1-55; col. 16, lines 7-21). The claimed global video bus which routes the video data between the processing module and the at least one video processing module and the claimed global control bus which is separate from the global video bus, and which provides control data to/from the processing module to the at least one video processing module is met by Gove, (col. 2, lines 52-64; col. 6, lines 11-39; col. 7, lines 25-65; co. 36, lines 4-27; col. 38, lines 34-64). In particular, the claimed global video bus reads on the crosspoint switch 20, which provides the parallel processors with video data memory 10 and the claimed global control bus reads on the communication bus 40, see Fig. 4.

Considering claims 2, 21 & 28, the claimed feature of crosspoint switch is met by the individual parallel processors' connection to the crossbar 20, (Fig. 1; Fig. 4; col. 6, lines 47-52; col. 7, lines 25-44). Gove does not specifically discuss a system clock, however such a feature which provides timing signals associated with video data is inherently included in Gove, which discloses that data is cycled through the various processors, in a synchronous or asynchronous manner (col. 3, lines 4-14; col. 6, lines 11-20; col. 12, lines 16-29). The claimed feature of timing signals which indicate that video data is active at least reads on the sync signal, which informs the processors that it is OK to execute code with respect attendant video data, (col. 21, lines 35-51).

Considering claim 3 & 24, the claimed state machine which monitors the transfer of video data and facilitates the allocation of paths for transferring among parallel processors, reads on the state machine 5708, included within the transfer processor 11, which monitors the block transfer of video data in the ISP nodes, (Fig. 57; col. 57, lines 61-67 thru col. 58, lines 1-21), in conjunction with the crossbar memories 10 and crossbar switch matrix 20.

Considering claim 20, the claimed method steps of creating a modular video processing system which corresponds with subject matter cited above in the rejection of claim 1, are likewise rejected. Regarding the additional claimed limitation of the parallel pipelined hardware being responsive to control data reads on Gove, (col. 13, lines 20-35). The further claimed limitation of the processing module detecting the presence of each video processing module connected to the global control bus, and passing the control data to each detected video processing module over the global control bus also inherently included in Gove, (col. 9, lines 35-31; col. 13, lines 20-35).

Considering claim 22, the claimed synchronous start signal reads on Gove, (col. 20, lines 1-12; col. 21, lines 36-50).

Considering claims 25 & 30, the claimed control data which comprises respective control signals for each hardware component of the video or specialized processing system, such that each processing module manipulates the control signals to program the instant hardware

components for each of the different specialized video processing operations corresponds to subject matter recited above in the rejection of claim 19, with respect to the hardware control library, and is likewise rejected.

Considering claim 27, the claimed features which correspond with subject matter recited above in the rejection of claims 1 & 20, are likewise rejected. Regarding the differences, the claimed at least one specialized processing module which contains parallel pipelined hardware that is programmable to provide different specialized processing operations on an input stream, reads on any particular ISP node, which contains a plurality of DSP processors which may currently perform different video processing operations on video data. The claimed general purpose microprocessor which has a hardware control library loaded thereon, wherein the hardware control library comprises a set of functions for programming the parallel pipelined hardware of the at least one specialized processing module such that the microprocessor performs predetermined specialized processing operations on the input data, reads on the operation of master processor 12, which comprises at least a register file 2901, opcode instructions 2911 and control logic 2904, which controls the microprocessor according to the instruction loaded. These instant loaded instructions enable the master processor 12 to schedule and control all video processing operations by the DSP parallel processors, (Fig. 29; col. 13, lines 20-37; col. 34, lines 53-64).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4 & 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove, in view of Kent, (U.S. Pat # 4,601,055).

Considering claims 4 & 26, in light of the 112 2nd rejection above, the claimed feature of dual image pointwise processing is interpreted as best understood by examiner, as dual portions of an instant image processed simultaneously. Gove teaches that in a parallel pipelined manner an image may first be received and processed by an image enhancement circuit or processor 1111, and sequentially received and processed by a plurality of other processors, i.e, at least 1110-1104 and 1109-1104, (col. 13, lines 60-67 thru col. 14, lines 1-55). However, Gove does not discuss the notoriously well known problem, that such a manner or pipelined processing may cause delay

between processors. Nevertheless, Kent discloses such a problem and presents, at least one delay compensation solution, (col. 6, lines 7-24; col. 10, lines 1-22). Thus it would have been obvious to one of ordinary skill lin the art at the time the invention was made to modify Gove, with the disclosure of Kent, providing delay compensation between image processing procedures for the well known benefit of efficient pipelined processing of images. Therefore, the claimed feature of a CALU which provides dual image pointwise operations and image accumulations reads on the combination of Gove, wherein multiple ISP nodes are disclosed, each which contains its own microprocessor thus can operate on an image, and Kent which provides delay compensation between pipelined image processors 10. Fig. 11, which relates to the disclosure of Gove cited above, teaches that dual portions of an image may receive simultaneous processing.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gove, in view of Sensar VFE-100, (Brochure).

Considering claim 5, Gove does not specifically discuss a pyramid filter processor which spatially filters video data at respectively different resolutions, however the claimed well known feature is disclosed by Sensar. It would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify the many parallel processors of Gove, which provide a variety of video processing functions, with the disclosure of Sensar, for the well known benefit of processing instant video data with multilevel processing.

8. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove, in view of Bilbrey, (U.S. Pat # 5,241,389).

Considering claim 6, Gove discloses in Fig. 1, that a plurality of parallel processors, i.e. DSP processors may be connected in an ISP node, but does not specifically state that the processors may be placed on separate daughterboards. However, the benefits of placing groups of circuits on a particular circuit board, which collectively provide a particular function were well known in the art at the time the invention was made. In particular, Bilbrey introduces a video processing system with a motherboard, and a plurality video processing subsystem cards 140, or daughterboards (Fig. 1; Abstract; col. 3, lines 46-60). Bilbrey teaches that the individual video processing subsystems 140, may provide different video processing functions, see (Fig. 2; col. 2, lines 40-50) and that the subsystems are connected via control data bus 120 and video data bus 150, (col. 3, lines 50-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to modify Gove with the disclosure of Bilbrey, to place individual ISP nodes, individual DSP processors or a plurality of DSP processors on a daughterboard connected to a motherboard for the known benefit of a more modular design, which at least allows an efficient means of replacing or repairing groups of circuits. Thus, modifying Gove to include one or more daughterboards, necessarily requires all pertinent connections of control data and video data transfer means between DSP circuits placed on the

instant daughterboards, and the memory banks & execution instructions which are already disclosed in Gove.

Considering claims 7-9, and regarding claim 7, Gove discloses a display processor means which formats video to a display means, 4803, (Fig. 46; col. 27, lines 11-15). As to the digitizer card, of claim 8, Gove discloses an A/D conversion means, 4904, (col. 28, lines 44-47; Fig. 49). As to claim 9, Official Notice is taken that correlator cards were well known in the art at the time the invention was made. It would have been obvious to one of ordinary skill lin the art at the time the invention was made to modify Gove & Bilbrey, with any number of DSP processing functions for the known benefits of specialized processing of the video image. Relying upon the argument presented above in the rejection of claim 6, with respect to placing video processing circuits on a daughterboard, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to place any circuit or group of circuits on a daughterboard, including the display means and A/D conversion means included in Gove, and a correlator card.

9. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove & Bilbrey, in view of Bruehl, (U.S. Pat # 5,051,835) and Purcell, (U.S. Pat # 5,809,174).

Considering claim 10, the claimed feature of placing various video processing circuits on a daughterboard, is rejected according to the analysis presented above in the rejection of claim 6.

Gove does not disclose a warper card, however, such a feature is shown by Bruehl, (col. 3, lines 40-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gove & Bilbrey, with the teachings of Bruehl, for the known benefits of graphics image processing, as taught by Bruehl. Even though the combination of Gove, Bilbrey & Bruehl do not disclose a bilinear interpolator, such a feature is taught by Purcell, (col. 26, lines 27-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination of Gove, Bilbrey & Bruehl, with the disclosure of Purcell, at least for the known benefits of more efficient pixel processing.

10. Claims 12-16, 17-19 & 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove, in view of Muramatsu, (U.S. Pat # 5,455,920).

Considering claim 12, Gove discloses in Fig. 3, a modular video processing system which may comprise a plurality of image processing systems, or ISP chip nodes, wherein the ISP chip nodes contain the circuits as shown in Fig. 1 & Fig. 2, which include a microprocessor as master processor 12, (col. 3, lines 39-44; col. 8, lines 51-66). One of ordinary skill in the art at the time the invention was made, would have readily recognized the benefit of utilizing a plurality of microprocessors in a particular system, in order to increase the productivity of the system, since different microprocessors would be enabled to at least operate on different instructions simultaneously. Recognizing such a benefit, Gove discloses at least one embodiment, in which in

addition to the master processor 12, one of the plurality of parallel processors 100-103, will act as the "master" processor and perform instruction fetches on behalf of all the other PP's, (col. 35, lines 58-67; col. 36, lines 47-67). However, even though Gove does not specifically disclose using more than one *microprocessor* in an ISP node, the technique of utilizing at least two microprocessors in one particular processing system, at least in a manner in which functions are shared or divided between the two instant microprocessors, which increases the speed and calculating capability of the instant system, was notoriously well known in the art at the time the invention was made, and is taught by Muramatsu, (Abstract; Fig. 1; 25-36; col. 1, lines 9-67; col. 2, lines). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Gove to include at least two microprocessors, as taught by Muramatsu, for the known benefit of improving the performance of a microcontrolled system. The claimed step of coordinating multitask operations of the two microprocessors is necessarily included in the combination of Gove and Muramatsu. Gove discloses that the plurality of ISP nodes may access a single global memory, (col. 8, lines 59-64). The claimed arbiter control bus is met by the bus 34, of Gove.

Considering claim 13, Gove discloses that the plurality of parallel processors may provide various video processing functions are begin execution based on the sync signal, (col. 9, lines 47-57; col. 20, lines 1-11; col. 21, lines 37-50; col. 42, lines 12-24; col. 60, lines 41-47).

Considering claim 14, Gove discloses that the video processors may receives input/output at least from a camera and display, which reads on a communication interface with external devices. The claimed arbiter control bus which controls access to the external devices from the plurality of processors is inherent in Gove.

Considering claim 15, Gove discloses that memory 10, associated with a particular microprocessor is connected to a global video bus, (col. 7, lines 16-22).

Considering claim 16, Gove introduces a system in which a plurality of microprocessors might be utilized to improve the performance of a modular video processing system. As noted above in the rejection of claim 12, the combination of Gove and Muramatsu provides a processing system with at least two microprocessors operating in conjunction, for the known advantages of a more efficient system. The claimed additional feature of a semaphore register, which at least facilitates the coordination of mutually exclusive operations by the instant at least two microprocessors, reads on the semaphores utilized by Gove, disclosed at least in the MIMD mode, (col. 41, lines 51-57).

Considering claim 17, regarding the claimed feature of a hardware control library which comprises functions for programming the parallel pipelined hardware to function concurrently, Gove teaches that the master processor 12 has access to all memory and operates the scheduling

and control of the entire system or node, (col. 13, lines 30-38; Fig. 29). Gove discloses that the different video processing procedures operate concurrently, (col. 9, lines 47-57; col. 20, lines 1-11; col. 35, lines 31-57).

Considering claim 18, Gove teaches that the plurality of ISP nodes, each of which may contain a microprocessor, operate concurrently, (col. 8, lines 63-67).

Considering claim 19, the claimed control signals which controls each hardware component, is inherent in Gove, (col. 8, lines 13-37).

Considering claim 23, the claimed method steps corresponds with subject matter rejected above in claim 16, and is likewise rejected.

Response to Arguments

11. Applicant's arguments with respect to claims 1-30, have been considered but are moot in view of the new ground(s) of rejection.

12. Applicant's arguments filed 6/7/99, with respect to the Muramatsu reference have been fully considered but they are not persuasive.

With respect to the Muramatsu reference, applicant argues on page 21, that the instant reference does not disclose signal processing operations being performed by the microprocessors. The examiner agrees and points that Gove is relied upon to teach such a feature. As discussed above in the rejection of claims 1 & 20, Gove teaches that the master processors 12, are microprocessors which also perform several video processing functions, (col. 13, lines 50-60). Therefore, Muramatsu is relied upon as a reference teaching the well known technique of operating two microprocessors in a particular processing system, which share processing functions and utilize a shared memory, thereby increasing the processing speed of the overall system.

Request for References

Applicant mentions on page 14 on the specification that the CALU may be implemented by the Xilinx XC4010FPGA or Xilinx XC4028. Examiner requests any information applicant can provide regarding the disclosed circuit, in order to fully understand the proposed invention.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's claims.

A) Taylor, Basoglu, Takeda, Guttag Parallel pipelined video processing system

B) Basavaiah Multi processing system with more than one CPU.

C) Winser Bilinear interpolator

D) Simpson State Machine

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 308-5399 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reuben M. Brown whose telephone number is (703) 305-2399. The examiner can normally be reached on Monday thru Friday from 830am to 430pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Faile, can be reached on (703) 305-4380. The fax phone number for this Group is (703) 308-9051.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4700.

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